MICROPROCESSOR BASED DATA ACQUISITION AND MONITORING FOR POWER SYSTEMS

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By

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CERTIFICATE

Certified that this work, 'MICROPROCESSOR BASED DATA ACQUISITION AND MONITORING FOR POWER SYSTEMS' by T.V. Prabhakar is carried out under our supervision and is not submitted for a degree elsewhere.

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ABSTRACT

This thesis is in two parts. Part I of the thesis deals with the design and implementation of a microprocessor based sub-station computer for data acquisition and monitoring of power systems. A data acquisition system consisting of sixteen analog inputs, eight digital inputs and a reference clock is built around Micro-78 - an eight bit microcomputer. System monitoring software which checks for alarm conditions (limits violation and status change) is developed. A teletypewriter acts as the man/machine interface and is used for display of alarms, system data and for logging. The performance of the system is checked on a sample power system simulated by a dc network analyzer.

Part II of the thesis deals with the requirements of energy control centres. These are discussed with particular reference to the U.P. State Electricity Board.

CHAPTER 1

INTRODUCTION

Since the first electric generator has been set spinning the demand for this form of energy has been growing at a fast rate. In modern society a disruption of electric supply could be catastrophic resulting in heavy losses to the economy and public inconvenience. It is the responsibility of the system operator to prevent such a disruption. He not only has to maintain continuity of supply but also its 'health' meaning the frequency and voltage should not deviate beyond specified limits. All this demands a co-ordinated control of the power system in conjunction with the neighbouring systems. At the control centre, the operator must be aware of the total system conditions in order to analyse and evaluate the current system status and to take if necessary any preventive measures to maintain the system security. This involves a system wide data acquisition network to gather and transmit data to the control, a digital computer to help process this large data and a system wide control network to execute the control strategy. These three units constitute the supervisory control and data acquisition (SCADA) network. A typical SCADA network is shown in Fig.1. Not included in this figure are various redundant structures (like a dual computer configuration) to increase reliability and reduce down time.

The advent of microprocessors made available low cost processing power. Microprocessors may be used in the SCADA network in places like peripheral processors and remote terminal units (RTU's). A peripheral processor is a data concentrator. It acquires data from the various RTU's in a multiplexed fashion, stores it, in a buffer memory and indicates to the central computer the availability of new data. This arrangement reduces the burden of scanning the communication channels for the central computer. A remote terminal unit forms the actual interface of the SCADA network to the power power system. Typically it is located in a substation and does the following functions:

(i) acquisition of analog bus voltages, line flows, generator outputs etc.

(ii) acquisition of digital inputs like circuit breaker positions.

(iii) activation of circuit breaker trippings, changing transformer taps etc.

(iv) transmission of system data to the central computer upon request or in a cyclic manner.

(v) driving local display equipments.

The incpropration of a microprocessor in an RTU extends its processing powers and makes the concept of a substation computer economically viable. With a programmable RTU/substation computer some amount of data processing

can be done at the sampling station itself. This allows a transmit on default option in the SCADA network (i.e. data is transmitted to the central control if and only if it has changed appreciably) reducing the burden on the communication network and also the errors that might crop up during transmission. In summary the functions that may be executed by a substation computer are:

(i) Acquiring the system data (analog and digital).

(ii) Limit checking and local alarm generation.

(iii) Driving of local recorders and other terminals (TTY's, CRT's etc.).

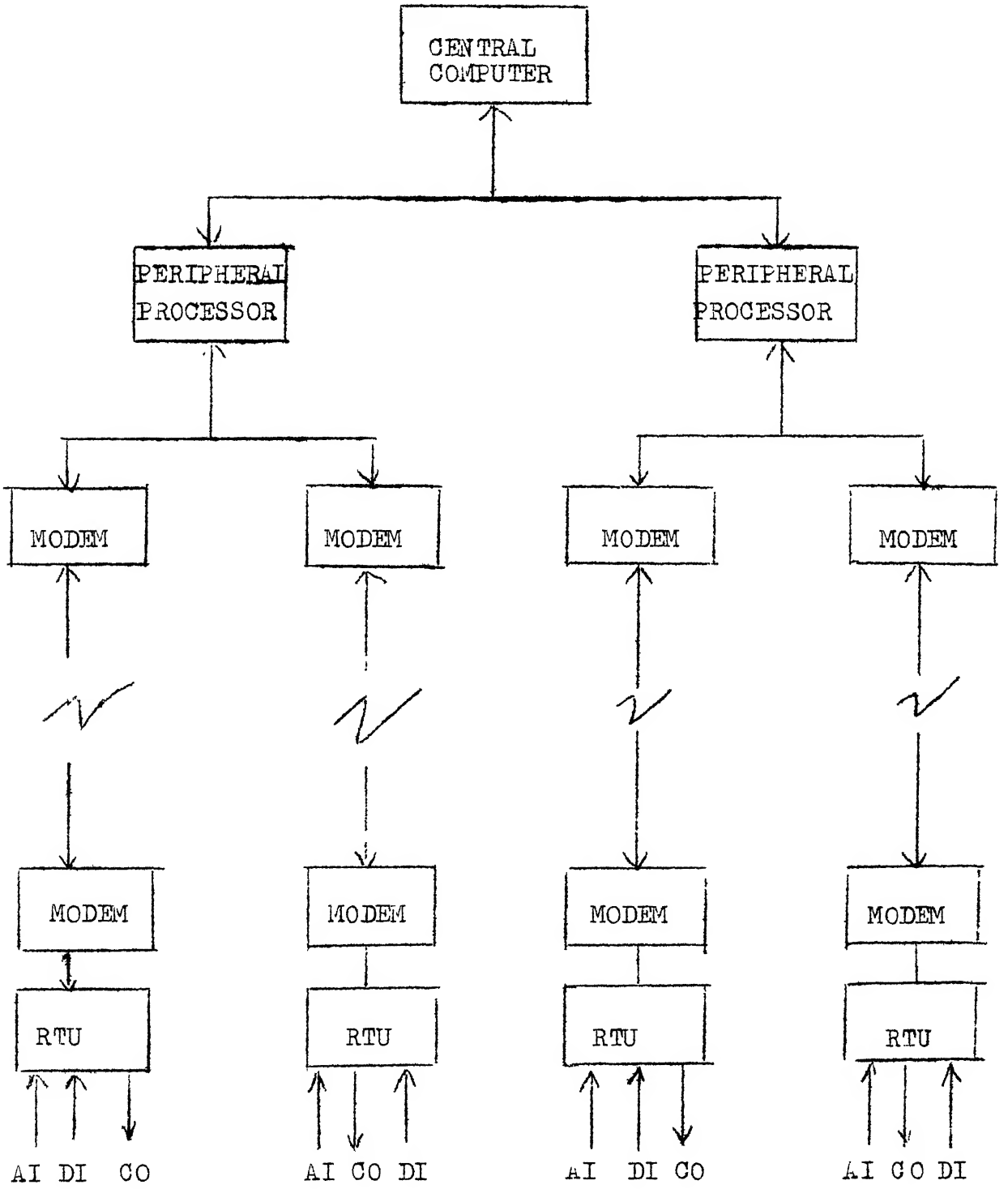
(iv) Handling the communication link with the central control (formatting, protocols etc.).

(v) Implementation of the control policy dictated by the central control.

It may be observed that the above summary does not include any 'protection functions' which are also important but not considered in this thesis.

This thesis is divided into two parts. The first part is devoted to the specification of a microprocessor based substation computer. This is discussed in Chapter 2. Chapters 3 and 4 give the hardware and software design respectively of the specified system. The performance of the designed system is evaluated in Chapter 5. The second part of the thesis as given in Chapter 6 is concerned with

giving the overall hardware/software requirements of an energy control centre at the state level. Finally, conclusions and scope for further work are given in Chapter 7.



AI : Analog Input; DI : Digital Input; CO:Control Outputs.

FIG.1.1 SCADA NETWORK.

CHAPTER 2

SYSTEM ORGANIZATION

The functions of a substation computer acting as a remote terminal unit in the SCADA network, to recall, are:

a) Reading in the current values of the analog and status inputs.

b) Limit checking and alarm generation.

c) Driving of local man/machine interfaces (CRT terminals, teletypewriters etc.).

d) Communication handling.

e) Execution of the control commands from the central control (open circuit breaker etc.).

A microprocessor based system was developed incorporating functions (a) to (c). Functions (d) and (e) were not included for want of a proper simulation environment and due to the magnitude of the problem involved. The system henceforth referred to as the Microprocessor Based Data Acquisition And Status Monitoring System (DASM) is built around an 8-bit microcomputer (Micro-78)* and is capable of accepting 16 analog and 8 digital inputs. These inputs are read in once every second and processed. A teletypewriter (TTY) serves as the man/machine interface. The operator can examine the value of any of the inputs through this TTY. The TTY is also used to display the alarm conditions in the system.

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* details of Micro-78 are given in the Appendix.

The functional specifications of the system are:

a) Read in the analog and digital inputs every second.

b) For the analog inputs - compare with preset upper and lower limits of the signal. If any limit is violated for 3 consecutive readings indicate so by printing a message on the TTY.

c) For the digital inputs - compare with the previous status and if it changes immediately indicate so by printing a message on the TTY.

d) Respond to operator display requests - the operator can ask any analog input value or digital input status to be displayed.

e) Real time clock - a software maintained real time clock which can be initialised at the time of starting.

f) Periodic logging - after every 10 minutes give a listing of the current system status and the peak values of the analog inputs since last listing.

The functional block diagram of the system is shown in Fig. 2.1. It consists of an analog input system, a digital input subsystem and a reference clock connected to Micro-78 through a general purpose interface. The details of each of these blocks are given in Chapter 3.

A dc network analyzer is used to simulate a small test system for the DASM to check and evaluate its performance. The single line diagram of the power system simulated is shown in Fig.2.2.

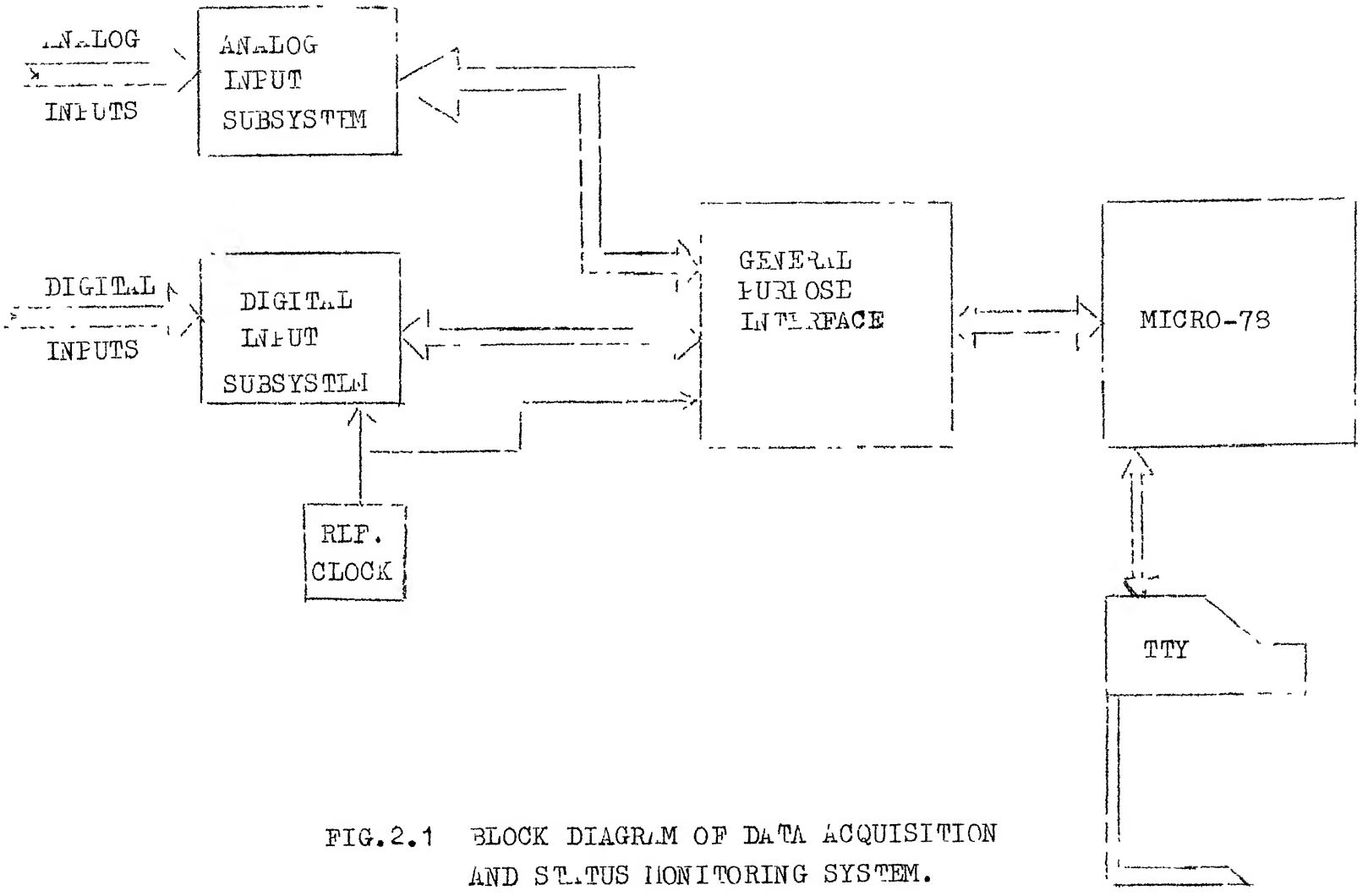
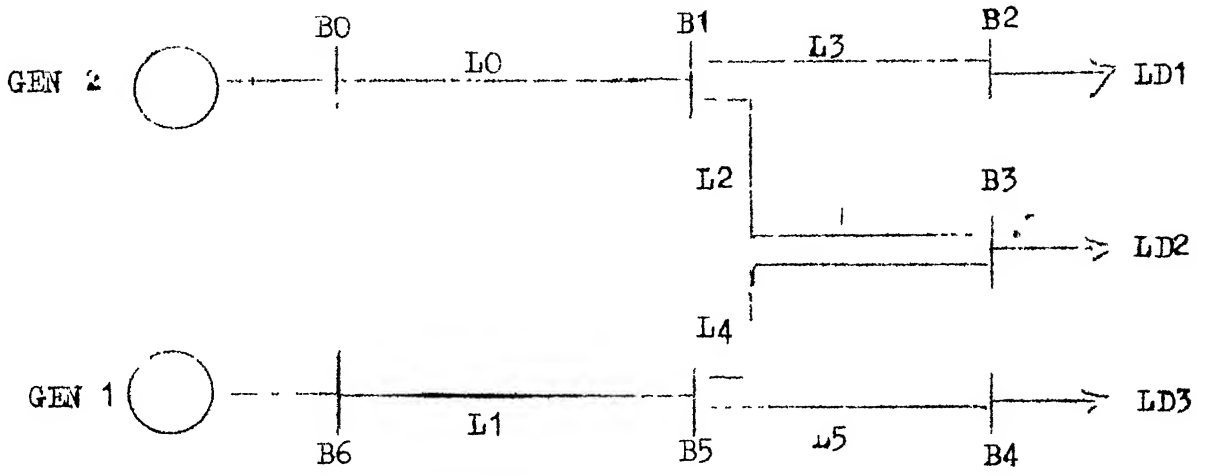


FIG.2.1 BLOCK DIAGRAM OF DATA ACQUISITION AND STATUS MONITORING SYSTEM.



B: Bus; L: Line; LD: Load

FIG.2.2 SINGLE LINE DIAGRAM OF THE SIMULATED POWER SYSTEM.

CHAPTER 3

HARDWARE DESIGN

The data acquisition and status monitoring system consists of an analog input subsystem, a digital input subsystem and a reference clock connected to Micro-78 through a general purpose interface. (Block diagram shown in Fig.2.1). This chapter describes in detail the functions of each of these modules.

3.1 GENERAL PURPOSE INTERFACE (GPI):

This consists of three I/O registers each of which is programmable either as input or output register by writing into a fourth register (status register). These four registers can be accessed by the In/Out instructions of the 8080 processor. The status register and the three I/O registers occupy contiguous locations in the 8080 I/O address space. This bank of (or four addresses) can be located anywhere from $0\text{-}377_8$ with the help of a DIP (dual-in line package) switch. The status registers will have the first address in the bank and the three I/O registers will have the rest of the three addresses. For example, if the last bank was selected in the address space (374-377) register 374 will be the status register and registers 375, 376 and 377 will be the I/O registers. Status register can only be written into. Bits 0, 1, and 2 in the status register determine the status (either input or output)

of the three registers 1, 2 and 3 respectively. A '1' in any of these bits makes the corresponding register into input mode. A '0' forces it into output mode. The rest of the 5-bits in the status register (bits 3 to 7) are not used. For example, if a pattern like xx xxx 101 is written into the status register 374, register 375 will be in input, register 376 will be in output and register 377 will be in input mode. The logic diagram of GPI is shown in Fig.3.1.

In output mode the data written into a register is latched and presented. Thus, data written into a register stays stable till it is written into again. The signals are taken out from a 44 PIN edge connector (.156" spacing). The pin configuration for this is shown in Fig.3.2.

The other features of the GPI are:

(1) With power on or Master clear all the registers go into input mode.

(2) For each register the read and write signals are also brought out. This enables the user to detect that a register has been written into or read from.

(3) An interrupt request line is brought out. This line must be driven low to interrupt the processor.

(4) A Master clear output is also presented which goes low with power on or Master clear to enable initialization of the user hardware.

The GPI circuitry is implemented on a Micro-78 standard sized printed circuit card and it occupies one slot in the Micro-78 cardcage.

3.2 ANALOG INPUT SUBSYSTEM (AISS):

This subsystem is to select,sample and convert the analog signals into digital equivalents. AISS can accept upto 16 single ended analog inputs and converts them into 12 bit binary form.

The heart of this subsystem is the BORR BROWNS SDM853 data acquisition module (DAC module). This module consists of an analog multiplexer instrumentation amplifier, sample and hold, analog to digital converter and the associated control circuitry in a single 76 pin package. Further details of this module are given in Appendix.

The component details of the AISS are shown in Fig.3.3. The DAC module is operated in a random assessible (normal) mode. This allows us to select any of the analog inputs by loading the corresponding address into th address register. The analog multiplexor is connected to enable any one of 16 analog inputs. The instrumentation amplifier is given a gain of x1 and the ADC is operated in the 0 - 10V range with 12-bit resolution. The A to D outputs are latched with the status signal coming from SDM853 and are presented to the GPI.

The AISS is accessed by Micro-78 through the general purpose interface. Registers 2 and 3 are used in input mode and register 1 isused in output mode. The least significant 4-bits (D0-D3) of register 1 are for channel selection and the most significant bit (D7) is to trigger the analog to digital conversion. The least significant bit in register 2 (D0) will indicate the status (end of conversion) of the ADC.

As shown in Figure 3.3, the MSBY of the ADC output (coming through the latch) is multiplexed with the 8-bits from the Digital Input Subsystem (DISS). This is to reduce the number of input registers required. Bit 6 (D6) of register 1 will allow us to multiplex these two signals.

Operating procedure of the AISS is as follows:

a) Select channel by writing its address into the least significant four bits of register 1.
b) Write a '0' and then a '1' on the MSB of register 1.
c) Wait till LSB of register 2 becomes zero.
d) Read-in register 3 (with D6 of register 1 as '0') and register 2.

3.3 DIGITAL INPUT SUBSYSTEM (DISS):

This subsystem consists eight D flipflops the inputs of which are fed from a voltage divider circuit. By choosing a suitable combination of R_1 and R_2 a '1' can be clocked into the flipflop if the signal voltage is above a certain value

and a '0' if it is below a certain level. R_1 and R_2 need to be choosen from the load it creates or the signal and the D flipflop input current limitations. A '1 sec. clock' which serves as a time reference to Micro-78 (as explained below) clocks the latest signal status into the D flipflops.

The reference clock has a frequency of 1 second and is used to maintain a real time clock through software. A D flipflop, set on the positive edge of the clock holds the interrupt line low till it is cleared by an acknowledge (coming as the read pulse of Register 2). The clock is obtained through a NE555 timer circuit. The logic diagram is given in Fig.3.3.

The analog input subsystem, digital input subsystem and the reference clock are implemented on a single printed circuit card and could be housed in the Micro-78 cardcage.

A small power system was simulated on a d.c. network analyzer and the DASM was used to 'monitor' the system. Single line diagram of the power system simulated is shown in Fig.2.2. The seven bus voltages and the status of the six transmission lines and two generators (ON/OFF) are read in every second and processed. Since a ON/OFF indication for the transmission line was not available the voltage at the middle of the line was used to determine whether a line is in circuit or not. Similarly the generator terminal voltage was sensed to decide whether the generator is ON or OFF.

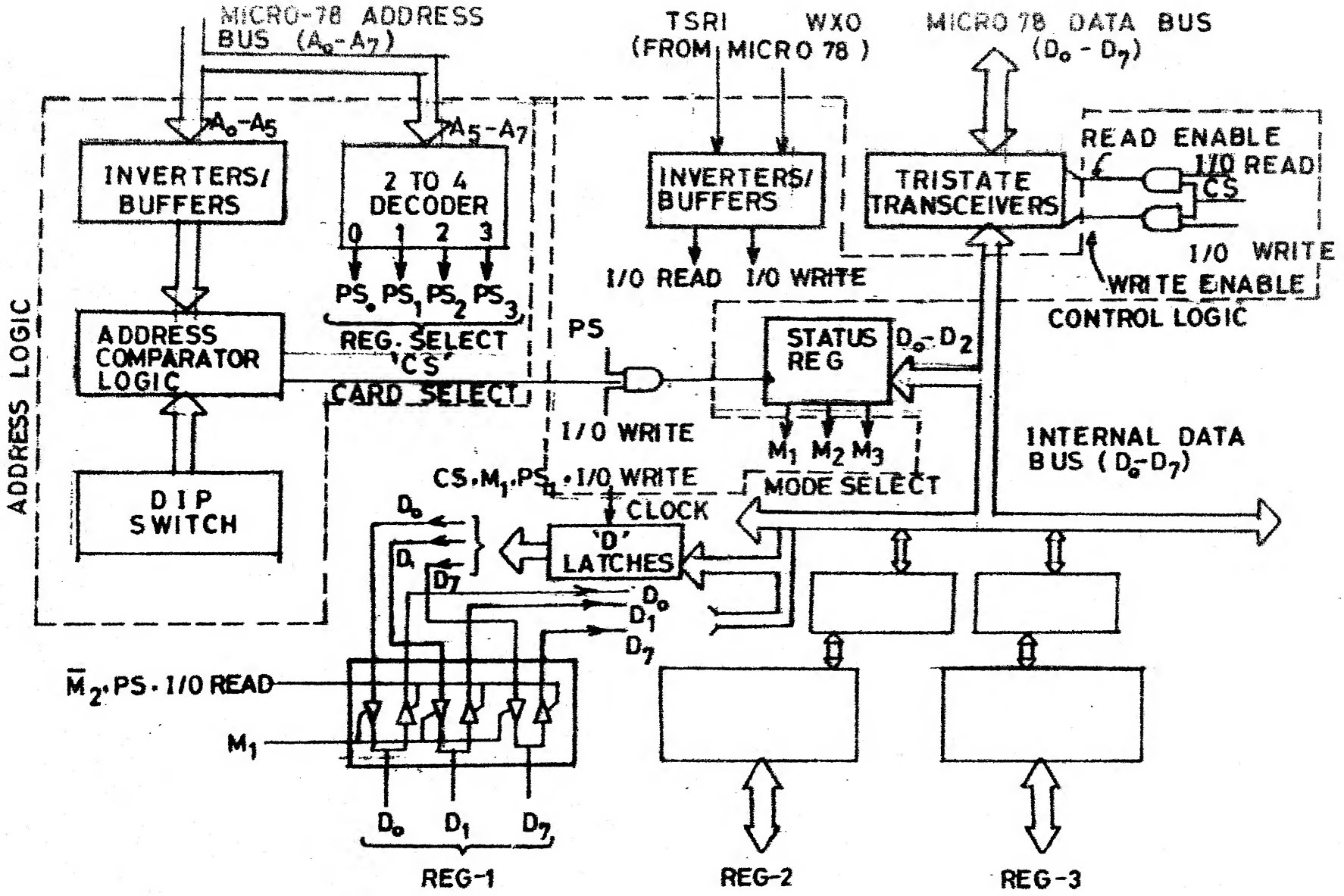
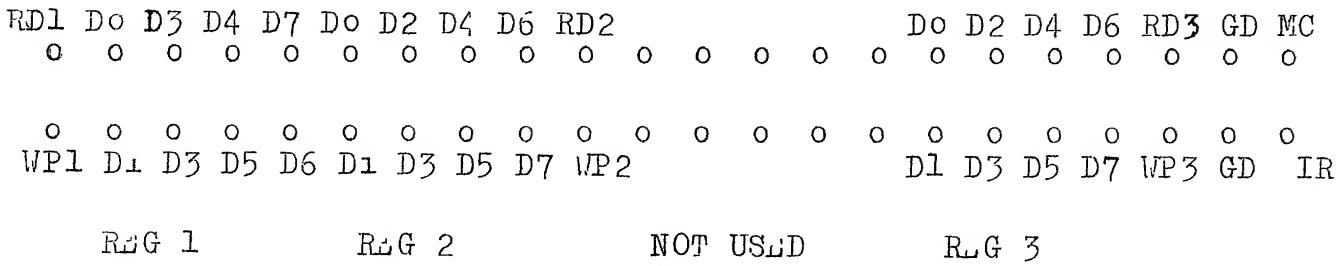


Fig.3·1 General purpose interface



44-PIN EDGE CONNECTOR
.156" SPACING

RD -READ PULSE
WP -WRITE PULSE
MC -MASTER CLEAR
IR -INTERRUPT REQUEST
PULL LOW TO INTERRUPT
GD -ground

FIG 3.2 EDGE CONNECTOR PIN CONFIGURATION

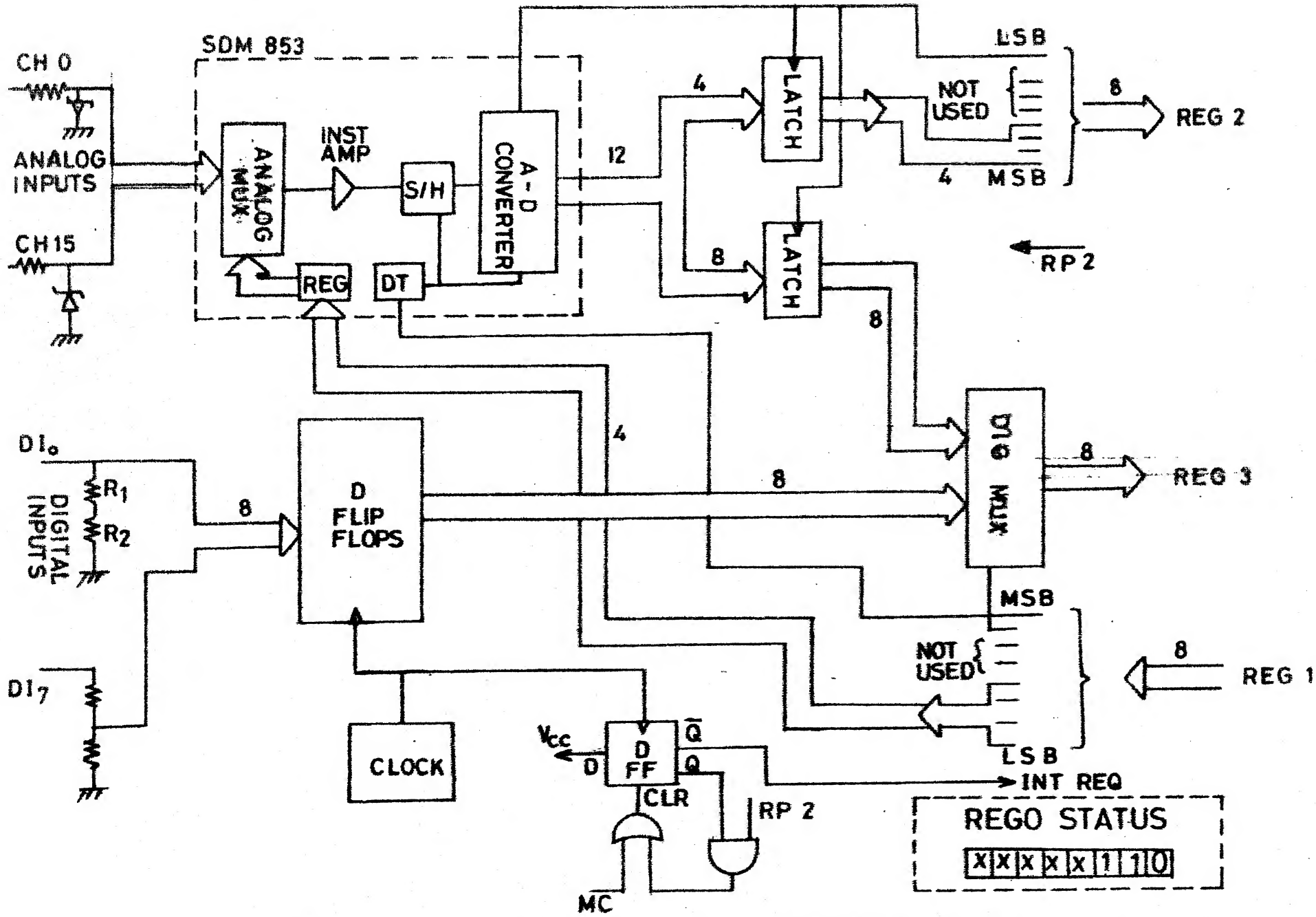


Fig. 3·3 Logic diagram of AISS+DISS+INT circuitry

CHAPTER 4

SOFTWARE DESIGN

The functions of the Data Acquisition and Status Monitoring system (DASM) in broad terms are:

a) Data acquisition and processing - This is a top priority function and is performed once very second. Here the analog and status inputs are read in and the alarm conditions are recognised. The output of this routine will be a set of alarm conditions or data to be communicated to the operator.

b) Alarms display - The alarm conditions recognised by the above routine are communicated to the operator by this routine. This will essentially mean printing out some data on the teletypewriter.

c) Operator display request monitoring - provides the system information requested by the operator.

These functions are described in detail below. This may be read in concurrence with the program description given in Appendix and flow charts of Figs. 4.1 and 4.2.

a) Data Acquisition and Processing - The CPU gets a 1 second reference signal through an interrupt. The processor has to see that the interrupt is enabled (by executing the EI instruction) as the 1 second interval approaches. The interrupt request line is held low by a

D flipflop till an interrupt acknowledge is received as a read pulse of Register 2. In Micro-78 there is only one level of interrupt. Upon receiving an interrupt the program counter is set to 70_8 after the completion of the execution of the current instruction. Identification of the interrupting device and allocation of priorities have to be done by software. However in the DASM there is only one interrupting device, that is the reference clock.

Since the data transfer rates are not high (16 channels, 2 bytes per channel) the acquisition of the 16 inputs is executed under complete control of the central processing unit. The cpu selects a particular channel, triggers the ADC, waits till end of conversion and then reads in the binary equivalents. The conversion time for each channel is about 33 micro seconds and the acquisition time for each channel is about 80 micro seconds.

b) Alarm displays: The teletypewriter which is used to display alarms is a slow I/O device. It can print about 10 characters per second. Since a single alarm might involve printing more than 10 characters, display of alarms generated in one scan might not be completed before the next scan. In order to avoid losing of alarms and at the same time not to miss any scans the following scheme is adopted. If any of the status inputs change their status, this information is entered into a First in First Out (FIFO) buffer called STATBUF.

Similarly on violation of upper or lower limits the alarms to be printed out are entered into another FIFO buffer called GENBUF. This is done by the interrupt service routine which does the data acquisition and processing function. Now program enters a dump loop where the STATBUF and GENBUF are emptied by a printing routine. The same is shown in the flowcharts in Fig. 4.1 and 4.2. The need for two FIFO buffers is explained latter.

c. Operator display requests monitoring: The operator can request any analog input or any status input position to be displayed. This he does by pressing appropriate keys on the keyboard. Then the CPU responds by filling the requested data in the GENBUF and jumping to Pt.1 in flow-chart of Fig.3.1. The operator might request all the analog inputs to be printed out in which case it takes more than 3-4 scanning intervals. Similarly at the end of every 10 minutes the system status and the maximum values recorded in that interval are printed out. This will encompass about 8-9 scanning intervals. In both cases if a status change is recognised during a scan its indication has to wait till the current printing is over if a single buffer is used. In order to give status change indication a higher priority in the printing queue it is entered into a different FIFO buffer STATBUF. In the dump routine even if the program is dumping the GENBUF it scans for STATBUF contents after printing each line. This is easily observed from flowchart in Fig.4.1.

The program has been written in assembly language and occupies an area of about 4000_8 bytes. An assembly language listing is given in the Appendix.

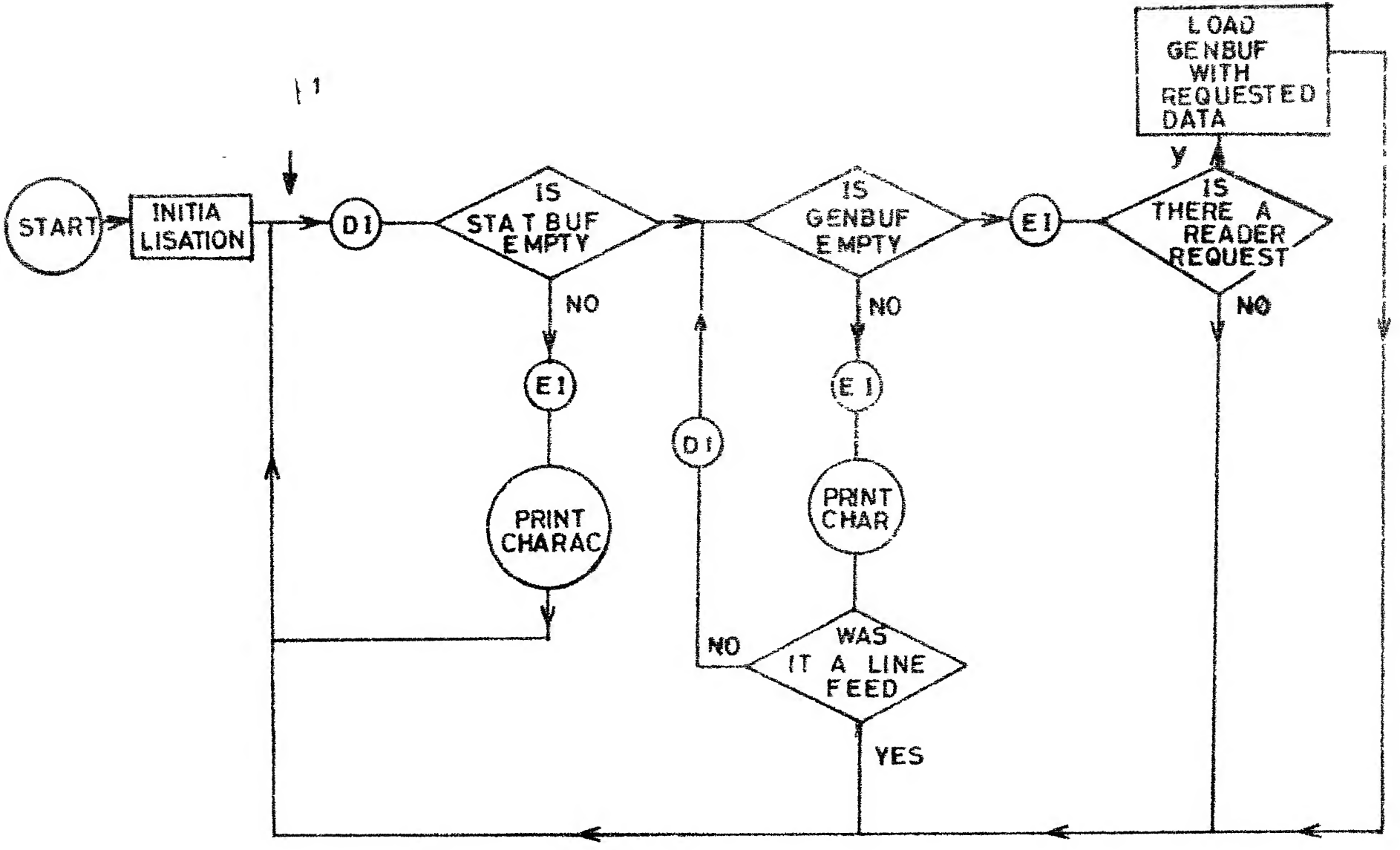
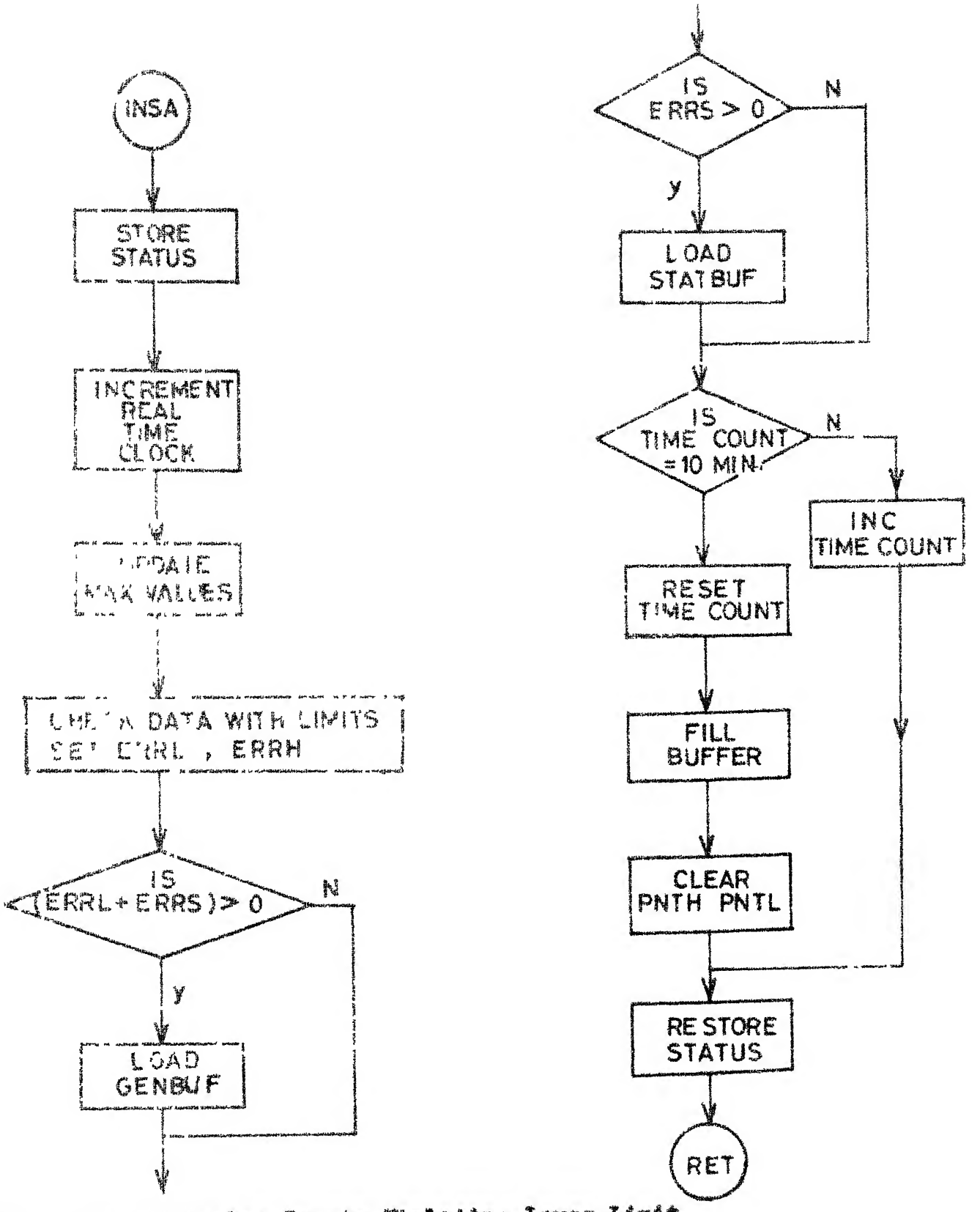


Fig.4·1 Dump routine



ERL : No. of Analog Inputs Violating Lower Limit

ERH : No. of Analog Inputs Violating Upper Limit

ERS : No. of Digital Inputs Changing Status

PNTH, PNTL : Pointers which Allow Display of a Violating Signal Only Once in 10 Minutes

Fig.4.2 INTERRUPT SERVICE ROUTINE

CHAPTER 5

PERFORMANCE EVALUATION

The data acquisition and status monitoring system was connected to a d.c. network analyzer which simulated a small power system and the performance was evaluated. The single line diagram of the simulated power system is shown in Fig.2.2. The simulated power system consists of two generators numbered 1 and 2, seven bus voltages numbered 0 to 6 and six transmission lines numbered 0-5.

The DASM was used to monitor the bus voltages, the line open/closed positions and the generator ON/OFF conditions. The generator voltages can be varied from 0-10V. All the bus voltages were given as analog inputs to the analog input subsystem(AISS). The analyzer does not provide any switch positions to indicate whether a line is in circuit or not. Hence the voltage at the middle of the line is sensed through the AISS and is used to recognize whether the line is OPEN or CLOSED. Similarly the generator output voltage is used to see if it is ON or OFF. The DASM reads in the system status every second and monitors the system. The various features of the system are described earlier in Chapter 2 and are again given below for easy reference.

a) Read in the bus voltages every second. If they exceed their upper or lower limits continuously for 3 seconds

print out the bus number, present voltage and the value of the limit exceeded. This indication of limit violation is given only once for each variable for each of the two limits in 10 minutes. This is done to avoid an irritating display of the alarm condition.

b) Read in line mid point voltages and the generator outputs and translate them to ON/OFF positions. If any of these inputs change their status indicate immediately by printing it on the teletypewriter.

c) Maintain a record of the maximum values of the bus voltages in a 10 minute interval.

d) Once every 10 minutes give a listing of the current system status (bus voltages and line and generator status) and the maximum values recorded for the analog inputs.

e) Permit the user to examine any bus voltage or line status (ON/OFF). The commands for these are described later.

f) Maintain a real time clock which can be initialized at start up.

Sample outputs of the system are given at the end of the chapter and are explained below in the order numbered.

Output 1: The operator wants to see the voltages on Bus 2. He presses D A 2 LF on the key board. Then the current, Bus2 voltage is printed. Similarly for Bus 3 voltage he has to press D A 3 LF and so on.

Output 2: If the operator likes to know the status of line 3 then he presses D S 3 LF . The system responds by printing the status of line 3. Similarly for lines 0, 1, 2, 4 and 5. Generators 1 and 2 can be addressed by D S 6 LF and D S 7 LF respectively.

Output 3: The operator can examine all the bus voltages by pressing D A $. The system responds by printing another $ and the bus voltages numbered 0 - 6.

Output 4: As in output 3 by pressing D S $ all the status inputs will be displayed.

Output 5: The operator has asked for a display of all the bus voltages. While the bus voltages are being printed Line 3 got opened. Since a change in status is an important event it should be immediately indicated to the operator. So the printing of the bus voltages is temporarily suspended, the change in status is indicated along with the time at which this occurred. After this the original printing is resumed and the rest of the bus voltages are printed. This facility has been arrived at by using two separate buffers for normal data display and status change display as explained in Chapter 4.

Output 6: A disturbance is created on the system by opening line 3. This is done by pulling out the jumpers which keep the line in circuit. This is indicated immediately by the processor. Also pulling out line 3 resulted in Bus 2 getting isolated. With the result its voltage came down and fell below the specified lower limit. This is also indicated by printing out the time at which this occurred, bus number, present voltage and the value of the limit violated.

Output 7: Line 3 which was open is put back in circuit. This is indicated again by the printed message.

Output 8: Bus 6 voltage is raised by increasing the Generator 1 voltage (This can be done by changing the pot setting). This, resulted in the voltage exceeding its upper limit. The message printed includes the time, bus no., present voltage and limit violated.

Output 9: The messages in this output explain the feature where the violating bus voltages are displayed only once every 10 minutes. When generator 2 is switched 'off' the bus voltages fall below their lower limits. The generator switching and limit violation is indicated immediately. Then the generator is switched 'on' which is intimated. When the generator 2 is switched 'off'

again before the 10 minutes interval only the switching information is conveyed and not the limit violation.

Output 10: This is a sample of the periodic logging done by the system. Once every 10 minutes (counted from the time the system is switched on) the system status is dumped along with the maximum values of the various inputs have taken in the 10 minutes interval.

The programs were developed in assembly language and run to about 4000_8 bytes of machine code and about 512 bytes of data. Under worst case conditions, the 'processing' part of the data might take about 150 m.s. (25000 instructions x 6 microseconds/instruction). Under quiscent conditions (no alarms, errors) the processing is through in about 50 m.s. Between two successive scans leaving this processing period the processor is free to handle the I/O devices. If sufficiently fast display terminals are used a lot of CPU time will be made available to implement more sophisticated functions.

Sample Outputs of the Data Acquisition and Status Monitoring System:

Output 1:

```
DA2
   2  4.759
```

Output 2:

```
DS3
   LINE 3  CLOSED
```

Output 3:

```
DA$$Ø  5.528
1  5.365
2  5.ØØ9
3  6.Ø68
4  6.944
5  7.215
6  9.579
```

Output 4:

```
DS$LINE Ø  CLOSED
LINE 1  CLOSED
LINE 2  CLOSED
LINE 3  CLOSED
LINE 4  CLOSED
LINE 5  CLOSED
GEN  1  ON
GEN  2  ON
```

Output 5: DA$$Ø 5.557

1 5.39Ø

1651 58

LINE 3 OPEN

2 5.Ø97

3 6.Ø89

4 6.962

5 7.233

6 9.579

1652 Ø4

LINE 3 CLOSED

Output 6: 1323 38

LINE 3 OPEN

1323 38

2 Ø.117V 4.664

Output 7: 1323 47

LINE 3 CLOSED

Output 8: 1324 Ø6

6 8.9Ø2V 8.783

Output 9: 1Ø3Ø 51

GEN 2 OFF

1Ø3Ø 51

Ø 3.587V 5.ØØØ

1 3.575V 4.976

2 3.373V 4.664

3 4.391V 4.664

Output 9 (continued):

1Ø3Ø 59

GEN 2 ON

1Ø31 Ø2

GEN 2 OFF

1Ø31 Ø7

GEN 2 ON

Output 10: 1654 3Ø

LINE Ø CLOSED

LINE 1 CLOSED

LINE 2 CLOSED

LINE 3 CLOSED

LINE 4 OPEN

LINE 5 CLOSED

GEN 1 ON

GEN 2 ON

Ø 5.289
1 5.143
2 4.852
3 5.924
4 6.851
5 7.118
6 9.566

PEAKS

Ø 9.483
1 9.262
2 9.162
3 9.262
4 9.614
5 9.570
6 9.698

CHAPTER 6

ENERGY CONTROL CENTRE DESIGN

Having seen in detail the functional specifications and implementation of a sub-station computer we shall consider the "central load despatch centre" or the "energy control centre" as it is called today.

The energy control centre is responsible for the integrated operation of the power system. The control strategy not only tries to maintain the power system in a secure mode but also attempts at minimizing the cost of operation. As of today, there are approximately about 80 control centres either in operation or nearing completion throughout the world. Given below is a summary of the various functions that are presently being carried out at the control centres.

a. Automatic Generation Control (AGC):

AGC means the regulation of the power outputs of the various generating stations so as to keep the frequency and tieline flows at specified limits. In most centres, this is the only major closed loop control being implemented. The sampling time for the AGC function varies from 1 to 4 secs.

b. Economic Despatch Calculation (EDC):

This function allocates the total desired generation among its different generating unit such that the system costs

incurred (fuel costs + transmission losses) are minimized. This function is performed every few minutes.

c. Automatic Voltage/Var Control (AVC):

This involves control of the reactive power generation/flows in the system to maintain the desired voltage profiles.

d. Security Monitoring (SM):

Security monitoring is the on-line identification and display of actual operating conditions of the power system. This one function has made the difference between the traditional despatch centre and the modern energy control centre. The SM function, in general, checks the analog values against limits basically to determine whether the system is close to, or at, the emergency state. This is done as often as the data is brought in which is usually in the order of one to a few seconds. SM also involves on-line determination of the network topology. A variety of display equipment like CRT's, dynamic display etc. are used by the SM function.

e. State Estimation (SE):

State estimation may be defined as a mathematical procedure for calculating, from a set of system measurements a 'best' estimate of the vector of bus voltage magnitudes and phase angles of the network. Benefits from SE include (a) bad data identification (b) calculation of non-telemetered

or missing data (c) establishment of base case for security analysis, and (d) better quality voltage readings. Typically the frequency of this routine is about 10-15 minutes.

d. On-line Load Flow (OLF):

An on-line load flow is a load flow run in real-time making use of real-time data. An OLF is used in functions such as security monitoring, security analysis and penalty factor calculations.

e. Steady State Security Analysis (SA):

The first function of security analysis (SA) is to determine whether the normal system is secure or insecure. The second function is to determine what corrective action should be taken when the system is insecure. The first function commonly known as contingency evaluation determines the security of the system with reference to a set of next contingencies. Determination of the corrective action is dictated to a large extent by the companies policy (like some companies might allow a system to be in an insecure state if the corrective action becomes 'too costly').

f. Optimum Power Flow (OPF):

An optimum power flow is a steady state solution to an optimisation problem where the load flow equations and limits on system variable constitute the set of constraints. This will become useful in producing a real-time data base for penalty factor calculation and security analysis.

g. Automatic System Trouble Analysis (ASTA):

ASTA is a logical procedure for analysing circuit breaker trippings and reclosings and protective relay operations. ASTA identifies (a) faulted circuits, permanent and temporary (b) primary and backup relay operations (c) breaker failures (d) breaker misoperations (e) primary relay failures (f) primary relay misoperations.

h. On-line Short Circuit Calculation (OSC):

OSC determines the maximum short circuit duty at each bus and compares with the switchgear rating. An alarm is generated when excessive short circuit duties are found.

i. Emergency Control (EC):

This is a closed loop control which automatically initiates load shedding, generation shedding, system splitting or line tripping in order to relieve overheads, to restore generation-load balance or to prevent cascading situations. The implementation of this function is still at a primitive stage in energy control centres.

j. Supervisory Control (SC): Supervisory control is a manual function. It allows the system operator to operate circuits breakers, regulate voltage control equipment or to start or stop a generating unit. It is implemented through the man/machine interface and comes to use as a manual type of emergency control.

It may be noted that as of now there is no single control centre which incorporates all the above listed functions.

An attempt was made in drawing up specifications of an energy control centre for Uttar Pradesh State Electricity Board (UPSEB). The results of the investigations are given below.

Uttar Pradesh is the most populous state in India. It has an installed capacity of 3000 MW and a connected load of 5000 MW. UPSEB is the only utility in India with a 400 KV transmission network. The state load despatch centre (SLDC) is located at Lucknow, the state capital.

For implementation of SCADA network the state is divided into three areas, eastern central and western U.P. Sahupuri, Lucknow and Roorkee will act as area control centres (ACC) for these three regions respectively. Each ACC will have a digital computer acting as a slave to the central control computer at Lucknow.

Utilities in developing countries face different problems to those in a developed country. In a country like India the demand usually exceeds the available generating capacity. The system operators main duty is the allocation (scheduling) of the available energy on a daily and monthly basis so as to minimize the amount of load shedding. This is in stark difference to an operator in

an advanced country who tries to allocate the generation among its various generating units to reduce the total generating costs. This factor forces the utilities in a developing country to justify the costs of the control equipment (which may have to be imported) solely on the basis of the operating facilities that become available. More often than not this is enough consideration to go for a computerised central control.

The energy control centre envisaged for UPSEB shall have the following features:

(a) Data acquisition
(b) Data validation
(c) AGC
(d) Alarm generation
(e) Data display
(f) Scheduling
(g) Load forecasting
(h) Logging
(i) State estimation
(j) Background processing.

These functions are executed by the SLDC computer with the help of the ACC computers. Given below are the respective roles of ACC and SLDC computers.

ACC: This is a slave station to the Master computer at SLDC. It duties are:

a) Acquire the power system data relevant to its own region.

b) Transmit area data to the central control.

c) Divide the area share of total state control error ($\Delta P_{tie} + k\Delta F$).among the participating generators in its own area.

d) Maintain the generator outputs at scheduled levels.

e) Local alarm generation.

e) Driving of local displays.

The ACC hardware might consist of (i) a microprocessor based processing unit (ii) a CRT screen to send/receive messages to SLDC and display of the area data and (iii) a logger to obtain hard copies of the messages and local alarms.

SLDC: This controls the area controls computers and is responsible for:

a) Data acquisition from ACC's.

b) Calculation of state control error ($\Delta P_{tie} + k\Delta F$) and dividing it between the areas.

c) Alarm generation.

d) Data display.

e) Data logging

f) Scheduling

g) Load forecasting

h) State estimation

i) Background processing.

The SLDC will require a 32-bit computer with reasonable processing power. The man/machine interface subsystem will include (a) Two alphanumeric cathode ray terminalswhich will be used for alarm display, data display and all other control functions. (b) A line printer for end of day logging, alarm logging etc. (c) A graphics terminal for single line diagram display. Other peripherals provided should cater to the needs of backgroundprocessing as well as providing standby for the on-line terminals.

The above listed functions are discussed now in detail.

(a) Data Acquisition:

The primary circuit in this function is formed by ACC's connected to the various sampling stations in the system. The SLDC will read in data from the ACC in the following manner. SLDC will send a data transmit signal to the ACC indicating the type of data required (like line flows,generator outputs or voltages). The ACC will transmit the required data to the SLDC only if those values have changed appreciably since the last transmission. Else it will indicate the SLDC of no change in the required values. The following could be the sampling rate at the SLDC level.

Sample	Frequency
MW,MVAR generations	1 sec.
Tie line flows	1 sec.
Circuit breaker status	1 sec.
Bus voltages	2 secs.
Energy meter readings	hourly
Reservoir levels	daily.

b) Data Validation:

This is done at the SLDC to ascertain the validity of the incoming data. Simple plausibility checks will be performed and non-conformity is indicated to the operator as an alarm message. For a non-conforming signal the previous value is retained in the data base. However, the operator can insert any desired value in place of the retained value. All the non- onforming signals are logged at the end of day. Upon detecting a non-conforming data coming from a particular area, the operator at the SLDC can transmit a message to the operator at ACC to initiate the necessary check procedures. Plausibility checks are performed as often as the data comes in.

c) Alarm Generation:

This is a security monitoring function which informs the operator of the vulnerable spots in the system. All the incoming signals are checked with their upper and lower limits and violation is indicated to the operator as an alarm which will be displayed on the CRT screen and has to be acknowledged. All alarms will be entered into an 'alarm file' which the operator can call for display. The operator will also be able to add/delete any alarm message in the alarm file. Similarly a change in circuit breaker status will also be given an 'alarm' status.

d) Automatic Generation Control:

This function is responsible for maintaining the tie-line flows (UP grid is tied to Bihar, M.P., Delhi and BBMB) and the system frequency at the scheduled value. The tie-line flows are monitored and transmitted to the SLDC by the respective ACC's every second. The SLDC calculates a state control error as $\Delta_{tie} + k\Delta F$. This is divided among the three regions, the ratios being determined by the regulating power available in each region. The ACC in turn will divide their share into individual generating shares and transmit to the generating stations. This function is performed once every 2 seconds. It may be noted that no ELD function is envisaged in the immediate future for want of enough generating power. However this feature can easily be incorporated into the present set by transmission of additional base point settings to the ACC by the SLDC. The ACC in turnwill maintain the generator outputs depending on these base point settings.

e) Data Display:

The display subsystem will consists of a graphics terminal and two alphanumeric terminals. The graphic terminal continuously displays the system one line diagram indicating the major transmission line and generating stations. This is refreshed only on request by the operator which permits him to study any configuration at his own

liesure. The diagram may be rolled up or down or to the sides to cover the whole grid.

The alphanumeric CRT's are the main interfaces between the operator and the computer. The two CRT's are perfectly identical but are driven independently. The CRT screen will be divided into two areas: top few lines reserved for the computer to indicate the operator that an alarm has been raised. The rest of the screen is devoted for the display of data requested by the operator. Typically an alarm condition might result in the following events. As soon as the alarm is recognised a message is flashed on to the top portion of the screen that an alarm has been raised and simultaneously an audible signal is set off. The operator responds by pressing on any of the CRT's a sequence of keys which acknowledge the alarm. Then the operator as soon as he is finished with the current data on display asks for the alarm to be displayed. This is displayed on the lower portion of the screen, which stays on till the operator deletesit. This way of dividing the screen into two areas allows the operator to study the data on display without annoyance and at the same time he does not miss any alarms. With the control CRT the operator can

a) request a particular bus voltage, line flow, CB status etc. to be displayed continuously and updated at every scan.

b) send a message to the operator at any ACC.

c) ask for any particular data to be printed out on the logger.

d) inspect/change the data base.

e) inspect/change the limits for alarm generation.

f) inspect the current hardware system status (are all the communication ckts. alright? etc.).

g) change the format of the various logs.

h) abort AGC function.

i) abort scan of any of the three ACC's.

j) receive any message from ACC.

) initiate/conduct diagnosis tests on the system.

l) allocate variables to the plotters (explained) below.

There will also be a few plotters (signal x time) whose input signal can be allocated by the operator. This will be of great help in system studies. The allocation of the signals is done through a control CRT.

(f) Logging:

A line printer will do the logging functions. The following types of logging is envisaged.

a) hourly logs indicating the current generation, tie-line flows, bus voltages etc.

b) End of day logging: summarizing the system performance in the past 24 hours.

c) Schedules suggested and followed.

d) Messages transmitted to and from SLDC and ACC.

e) Any otherdata requested by the operator through the control CRT.

g) Scheduling:

Once every day the generation and tie-line schedules are calculated and after approval by the SLDC operator are entered into the data base. These schedules are also transmitted to ACC's which will control the individual generator outputs at the scheduled level. The scheduling is done with the help of the following information:

a) previous day's actual generation

b) previous day's system load curve

c) annual generation schedule

d) annual maintenance schedule

e) load forecast for the coming 24 hours

f) contingencies that might have come up in the last 24 hours

g) any other information as desired by the operator.

h) Load Forecasting:

Once every day the expected load curve is calculated from the last day's load curve and other relevant data. This forecast is updated every 30 seconds. The forecast helps the system operator to get ready in meeting any excessive demand.

1) State Estimation:

This is a function whose usefulness will not be obvious for an electric utility of UPSEB's nature where the control centre functions are oriented towards 'management of a real time data base'only. However, this is included with the expectation that it will help isolate faulty meters and erroneous communication links. This function could be run once every 30 minutes or so.

3) Background Processing:

This is a very desirable facility for an energy control centre. This essentially means the computer sub-system is available for off line program execution when not doing any real time computation. In a dual computer configuration the second computer which is a hot standby for the computer"on-line"will be used for background processing. For the UPSEB control centre a dual computer complex is envisaged with the standby computer providing background processing. Also a simulator program may be made available with a control CRT similar to the on-line one so that operator training can be carried out.

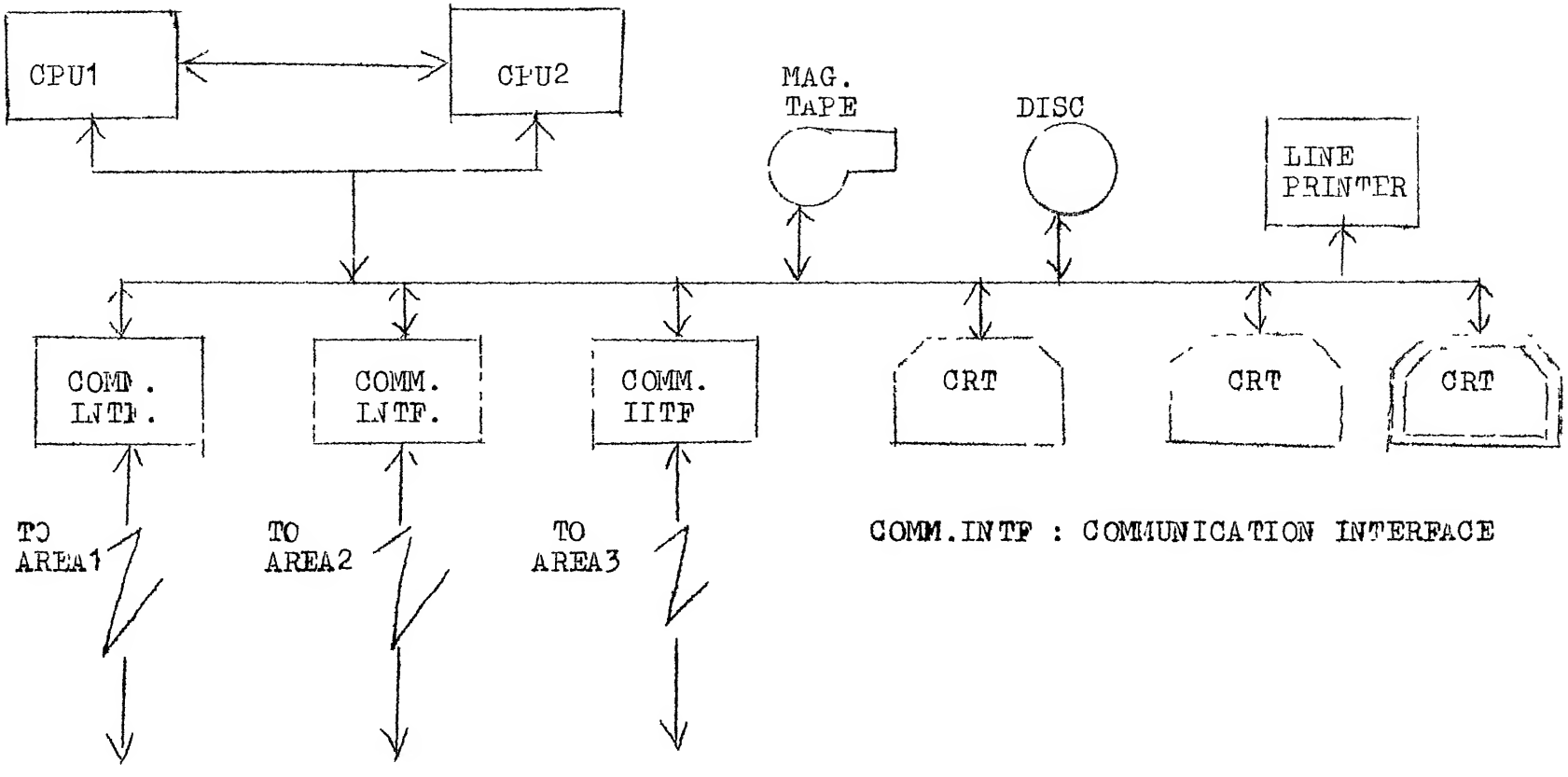


FIG.6.1 SLDC HARDWARE CONFIGURATION.

CHAPTER 7

SCOPE FOR FURTHER WORK

The first part of the thesis described the design and implementation of a data acquisition and status monitoring system. The system was configured with available resources in a time bound atmosphere. With the result many desirable features had to be left out. Some of them are discussed below.

(a) A teletypewriter was used as the man/machine interface. All the alarm displays, logging etc. was done through this. A teletypewriter is a very unsuitable form of display device for our application. A more appropriate I/O device is a CRT terminal. A CRT terminal allows us to provide a continuous display of the system variables. Alarm messages can be displayed by making appropriate parts of the screen blink. If graphic facilities were also available on the CRT, a display of the single line diagram of the system being monitored can be provided.

(b) The display facilities in our system are very limited. The operator can only examine the current values of the analog and digital inputs. It would also be very helpful to know the previous values of the signals. This can be easily implemented by maintaining a history file for each of these inputs. Other forms of display like trend display can also be implemented.

(c) Another important function that substation computer can implement is event recording. This involves maintaining

a historical file of fixed length (say 60 seconds) for each input, update it with every scan, freeze it on observing a fault in the system, store the signal level for the next 60 seconds and provide this set of prefault and postfault data to the system operator. This will be very helpful in fault analysis.

(d) The second part of the thesis describes a sample design of an energy control centre for UPSEB. Further work could be done on this problem and could consist of

a) Specification of the exact sampling points on the system.

b) More detailed specifications of the computer subsystem (computing power, operating system etc.).

c) Utility software design - implying determination of

   i) algorithms to be used in the system functions like state estimation etc.

   ii) different display formats, modes of creating and changing formats etc.

   iii) phased approaches for implementing the overall system functions.

REFERENCES

1. Micro-78 - Systems Reference Manual: ECIL Hyderabad.
2. SDM 853 Users Manual - Burr Brown Corporation, U.S.A.
3. 8080 Users Manual - Intel Corporation, U.S.A.
4. The TTL Data Book for Design Engineers - Texas Instruments Corporation.
5. Tomas E. DyLiacco - Tutorial on 'Energy Control Centre Design': IEEE Press Publication.
6. Tomas E. DyLiacco - System Security: The Computers Role: IEEE Spectrum, May 1978.
7. Russel & Council - Power System Control and Protection: Book, Published by Academic Press.

APPENDIX A

SDM 853 - DAC MODULE

SDM 853 contains all components necessary to multiplex and convert upto ±10V analog data into equivalent digital outputs at throughput sampling rates of 30 kHz for 12 bit resolution and 43 kHz for 8-bit resolution. Fig. A.1 gives the component details of SDM 853.

The analog multiplexor consists of two integrated CMOS circuits. Two of eight or one of 16 analog inputs may be switched to common outputs with a digital control input. Input selection is accomplished by four binary address inputs. The counter serves as an address storage register for the selected analog input. The delay timer is a non-stable multivibrator and is adjusted for a time interval of approximately 9 microsecs. After a new channel has been addressed this time interval is used as a delay to allow the multiplexor, instrumentation amplifier and sample/hold cifcuit to settle to a new value. The instrumentation amplifier gain can be programmed by an external resistor for gainsfrom x1 to x1000. Sample/hold normally tracks the outputs of the instrumentation amplifier. During an analog to digital conversion the circuit holds the value at its inputs at the time conversion begins. This Sample/hold circuitry allows analog input data to be sampled with time uncertainty of approximately 5 nano sec. The analog to digital converter can be operated with input voltage ranges of 0 to +5, 0 to +10,

-2.5 to +2.5, -5 to +5 and -10 to +10 volts. Conversion time is approximately 24 microseconds for 12 bit resolution. A short cycle facility allows operation at lower resolution and correspondingly higher speeds.

The system can be operated in two basic modes - normal and overlap. In normal operation the channel address is loaded or clocked into the address counter. The addressed channel will remain selected during its analog to digital conversion. In overlap mode channel N+1 is selected while channel N is being converted. This can be used to increase the system throughput rate by allowing the multiplexor and instrumentation amplifier to settle while a conversion is being made. In this way the throughput rate is limited by the sample/hold acquisition time and the analog to digital converter conversion time.

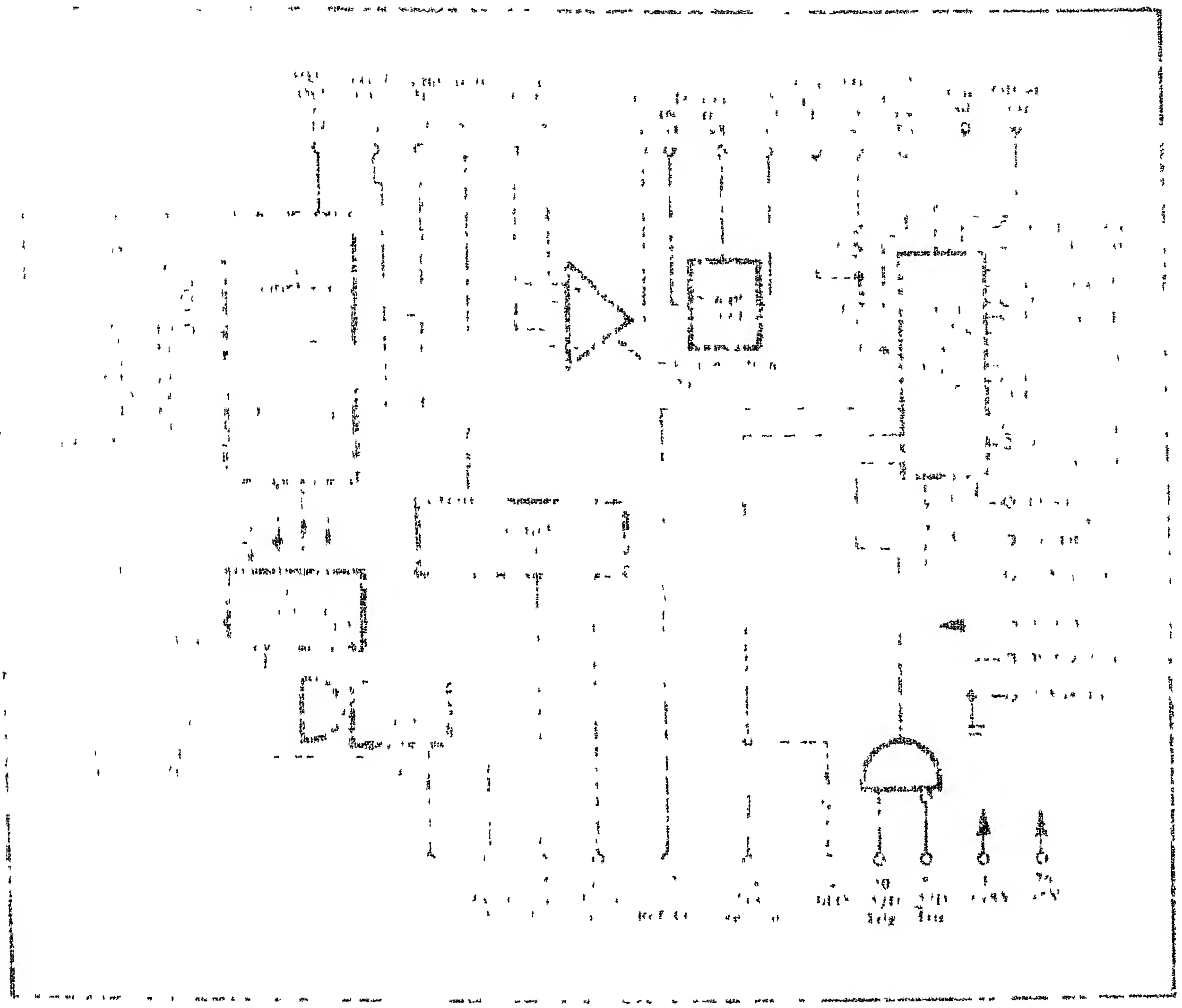


FIGURE [illegible]. [illegible] DETAIL [illegible] 652.

APPENDIX B

MICRO-78

Micro-78 is an 8-bit microcomputer with Intel-8080A as the central processing unit. It has a machine cycle time of about 2 micro-seconds and can directly address upto 64K bytes of memory. It has 256 input and 256 output ports through which it communicates with the various peripheral equipment like Teletypewriter, CRT terminal etc.

The standard system software includes a basic assembler, an On-line Debugging System, a variety of utility packages and mathematical routines and 'Basic' language interpreter. A cross assembler and simulator written in Fortran IV are available as standard support wsoftware.

Micro-78 I/O bus consists of 33signals and these are described below.

S.No.	Name	Description	Logic	No.of lines
1.	Add_0 to Add_{15}	Address lines from CPU to Memory and I/O gives the memory address in case of memory or DMA operations. Add0 to Add7 specifies port address for I/O operations.	-ve	16
2.	D_0 to D_7	Bidirectional Data bus. Carries the memory data for memory read/write operations and input/ output data to memory in case of DMA operations.	-ve	8

S.No.	Name	Description	Logic	No. of lines
3.	WXM	Write pulse for memory. With this pulse the memory storbes the data from CPU or in case of DMA from I/O. This signal is removed by SSYN.	-ve	1
4.	WXO	Write pulse for I/O. With this pulse the output strobes data from CPU. This pulse is 0.48 to 2 micro-seconds- typically about 1.5 micro sec. Data can be strobed at any time during this pulse including both the edges.	-ve	1
5.	TSRM	Read pulse for memory. With this pulse the memory gates the data on Data in bus of the CPU or in case of DMA to the I/O.	-ve	1
6.	TSRI	Read pulse for I/O. With this pulse the I/O should gate the data to CUP Data in bus.	-ve	1
7.	SSYN	This is a synchronising signal from Memory, indicating that a memory read/write is completed.	-ve	1
8.	IR	Interrupt request indicates that one or more device is requesting to interrupt the CPU	-ve	1
9.	DMAR	DMA request indicates that a DMA device is requesting to interrupt the CPU	-ve	1
10.	DMAA	DMA acknowledge acknowledges that a valid DMA request has been received by the CPU. This signal is removed soon after the DMA request is removed by I/O.	-ve	1

S.No.	Name	Description	Logic	No. of lines
11.	MC	This is a Master Clear signal issued by the CPU to initiate some flags and registers in the device controllers.	-ve	1

All these signals run parallely on the back panel mother board in the Micro-78 cardcage. The following are the pin numbers for these signals. (Bottom row odd and top row even. Start counting from left. Left leg is a middle one is b and right leg is c).

Signals	Pin No.	Signal	Pin No.
Add_0-Add_{15}	a_1 to a_{16}	TSRM	a_{25}
D_0 - D_7	a_{17} to a_{24}	WRM	a_{26}
SSYN	a_{27}	MC	a_{28}
TSR_I	a_{29}	WXO	a_{30}
Int. Req.	a_{31}	DMA Req.	a_{32}
DMA Ack.in	a_{34}	*DMA Ack.out	a_{33}

*NOTE (1): The devices which do not use DMA should short the pins a_{33} and a_{34} on the respective cards.

(2) The assorting of DMA request should be conditioned with DMA ACK not present.

The following pins are for the different bus voltages.

Voltage	Pin	Voltage	Pin
+5V	a_{39}, b_{39}, c_{39}	-5V	C_1: GND C_2
-12V	C_5 : GND C_6	+12V	C_9: GND C_{10}
- 9V	C_{13}: GND C_{14}	+20V	C_{17}: GND C_{18}

GND + 5V a_{40}, b_{40}, c_{40}.

APPENDIX C

DESCRIPTION OF THE DATA ACQUISITION AND PROCESSING PROGRAM

Micro-78 willusually be executing DUMP routine. Upon an interrupt it goes to INTERRUPT SERVICE ROUTINE(INSR) and returns back.

DUMP ROUTINE

1 READ TIME FROM CONSOLE AND STORE IT IN MEMORY

2 SET PNTH, PNTL TO ZERO

3 INITIALISE STATBUF POINTER AND GENBUF POINTER

4 DISABLE INTERRUPT

5 TILL STATBUF IS EMPTY DO

   a. Retrieve a character from STATBUF

   b. Enable Interrupt

   c. Print that character

   d. Disable Interrupt

   e. Increment STATBUF pointer

6 TILL GENBUF IS EMPTY DO

   a. Retrieve a character from GENBUF

   b. Enable interrupt

   c. Print that character

   d. Disable interrupt

   e. Check if the character printed was a line feed. If Yes do f. Else Do g

   f. Go To 4

   g. Increment GENBUF pointer

7 ENABLE INTERRUPT

8 IS THERE A READER REQUEST? IF YES GO TO 10. ELSE GO TO 2

9 GET THE CHARACTER FROM TTY. IS IT A D? IF YES GO TO 10. ELSE GO TO 12.

10. READ THE NEXT CHARACTER FROM TTY. IS IT AN A? IF NO GO TO 11. ELSE DO

a. Read another character from TTY

b. Is it a $? If yes load all the analog voltages in GENBUF and go to 3. If not continue.

c. Is it a ','? If yes go to 3. Else (it will be a number) load GENBUF with appropriate analog voltage and go to a.

11. IS IT A S? IF NOT GO TO 3. ELSE

a. Read next character from TTY

b. Is it a "? If yes load all the current status input positions in GENBUF and go to 3. Else continue.

c. Is it a ','? If yes go to 3. Else (it will be a number) load GENBUF with corresponding input status and go to a.

12 IS IT A #? IF YES GO TO 1. ELSE GO TO 3.

INTERRUPT SERVICE ROUTINE (INSR)

1. STORE REGISTER CONTENTS IN THE STACK
2. INCREMENT THE REAL TIME CLOCK BY 1 SEC
3. FOR ALL 7 ANALOG INPUTS
    a. Output channel number
    b. Trigger ADC
    c. Wait until end of conversion
    d. Read in the binary number and store in memory.
4. FOR ALL 8 STATUS INPUTS
    a. Output channel number
    b. Trigger ADC
    c. Wait until end of conversion
    d. Read in the binary number and store in memory.
5. CLEAR ERRS, ERRL, ERRH
6. FOR ALL 8 STATUS INPUTS
    a. If voltage is greater than 1.25V set status = closed else set status = open.
    b. Compare it with previous status if equal do g else do c.
    c. Increment ERRS. Load variable number into TABS table.
    d. Continue.

7. FOR ALL 7 ANALOG INPUTS

   a. Compare with preset upper limit. If greater do b. Else reset 'FLGH' and do e.

   b. Increment 'FLGH' flag. If equal to 3 reset FLGH and do c. Else do e.

   c. If 'PNTH' flag is set do e. Else set PNTH and do d.

   d. Increment ERRH. Load variable number in table TABH.

   e. Continue.

8. FOR ALL 7 ANALOG INPUTS

   a. Compare with preset lower limit. If less do b. Else reset FLGL and do e.

   b. Increment 'FLGL' flag.If equal to 3 reset FLGL and do c else do e.

   c. If PNTL is set do e. ELSE set PNTL and do d.

   d. Increment ERRL. Load variable number in table TABL.

   e. Continue.

9. FOR ALL 7 ANALOG INPUTS

   a. Check with present peak values. If greater do b. Else do c.

   b. Store current value as peak.

   c. Continue.

10. INITIALISE POINTERS TO TABLES TABS, TABH AND TABL.

11. FOR ERRS GREATER THAN ZERO DO

    a. Retrieve variable number from table.

    b. Retrieve corresponding status from current status buffer.

    c. Load variable number and current status in STATBUF

    d. Increment table pointer and decrement ERRS

12. FOR ERRH GREATER THAN ZERO DO

    a. Retrieve variable number from table

    b. Retrieve voltage (in binary) from current data buffer and convert to decimal equivalent

    c. Retrieve corresponding upper limit (stored in binary) and convert it into decimal.

    d. Load GENBUF with variable number, current voltage and upper limit.

    e. Increment table pointer and decrement ERRH.

13. FOR ERRL GREATER THAN 0 DO

    a. Retrieve variable number from table TABL.

    b. Retrieve corresponding voltage (which is in binary) from current data buffer and convert to decimal.

    c. Retrieve corresponding lower limit (stored in binary) and convert to decimal.

    d. Load GENBUF with variable number, current voltage and lower limit.

    e. Increment table pointer and decrement ERRL.

14. INCREMENT INTERVAL TIME COUNT. IF EQUAL TO 10 MIN. DO 15. ELSE DO 16.

15. LOAD INTO GENBUF TIME, ALL ANALOG VOLTAGES, DIGITAL STATUSES AND PEAKS RECORDED IN PAST 10 MIN. CLEAR PNTH AND PNTL.

16. RESTORE REGISTER CONTENTS FROM STACK.

17. RETURN.

NCHS : No. of digital signals that changed their status.

NHGH : No. of analog signals violating their upper limits.

NCHL : No. of analog signals violating their lower limits.

TABS : Table containing the signal numbers that have changed status.

TABH : Table containing the signal numbers that have violated their upper limits.

TABL : Table containing the signal numbers that have violated their lower limits.

FLGH : Indicates no. of violations of upper limit.

FLGL : Indicates no. of violations of lower limit.

PNTH : If zero allows display of upper limit alarm signal. Set by first violation. Reset every 10 minutes.

PNTL : If zero allows display of lower limit alarm signal. Set by first violation. Reset every 10 minutes.

STATBUF: A FIFO buffer containing status change alarm signals.

GENBUF: A FIFO buffer containing 'limits exceeded' alarm signals and other data to be displayed.

ASSEMBLY LANGUAGE LISTING

```
INIT:NOP
     MVI  A,200B
     OUT  375B
     MVI  B,110B
     LXI  H,REFS
     XRA  A
BNIT:MOV  M,A
     INX  H
     DCR  B
     JNZ  BNIT
     STA  CHPT
     STA  LRTP
     LXI  H,0
     SHLD TCNT
     LXI  H,16000B
     MVI  M,44B
     SHLD BSAF
     LXI  H,16300B
     MVI  M,44B
     SHLD BFAF
     LXI  H,TIMH
     CALL CRAP
     DCX  H
     CALL CRAP
     DCX  H
     CALL CRAP
CNIT:CALL READ
     CPI  15B
     JNZ  CNIT
DUMG:IN   376B
     EI
     NOP
     EI
     NOP
DUMS:CALL ZANG
DUMB:NOP
     LXI  H,16300B
LUMP:DI
     NOP
     MOV  A,M
     CPI  44B
     JZ   PUMP
     INX  H
     MOV  C,A
     EI
     NOP
     EI
     NOP
     CALL PRIN
     DI
     NOP
```

```
      MOV A,C
      CPI 12B
      CZ ZANG
      JMP LUMP
PUMP:LXI H,16300B
      MVI M,44B
      SHLD BFAF
      EI
      NOP
      EI
      NOP
RDRC:IN 10B
      ANA A
      JP DUMS
      IN 11B
      MOV C,A
      CPI 104B
      JNZ RUSK
      CALL GITA
      JMP DUMS
RUSK:CPI 103B
      JNZ BRTN
      CALL CHNG
      JMP DUMS
BRTN:CPI 43B
      JZ INIT
      CALL PRIN
      JMP DUMS
      NOP
      NOP
      NOP
INSF:PUSH B
      PUSH D
      PUSH H
      PUSH PSW
      IN 376B
      ANI 002B
      JNZ ANSR
      MVI B,61B
      CALL ERPT
      HLT
ANSF:NOP
      LDA CHPT
      ANA A
      JZ BNSR
      MVI B,62B
      CALL ERPT
      HLT
BNSI:MVI A,377B
      STA CHPT
RTC:LXI H,TIME
      MOV A,M
      INR A
      DAA
      CPI 240B
      MOV D,A
      JNZ ARTC
```

```
      MVI  D,Ø
      INX  H
      MOV  A,M
      INR  A
      DAA
      MOV  E,A
      CPI  240B
      JNZ  BRTC
      MVI  E,Ø
      INX  H
      MOV  A,M
      INR  A
      DAA
      MOV  C,A
      CPI  5ØB
      JNZ  CRTC
      MVI  C,Ø
      NOP
CRTC:MOV  M,C
      DCX  H
BRTC:MOV  M,E
      DCX  H
ARTC:MOV  M,D
      NOP
DAC:LXI  H,DATA
      MVI  B,Ø
BDAC:MVI  A,Ø
      ADD  B
      OUT  375B
      ADI  2ØØB
      OUT  375B
ADAC:IN 376B
      RRC
      JC ADAC
      RLC
      CMA
      ANI  36ØB
      MOV  D,A
      IN 377B
      CMA
      MOV  M,A
      INX  H
      INR  B
      MOV  M,D
      INX  H
      MOV  A,B
      CPI  2ØB
      JNZ  BDAC
      NOP
      XRA  A
      STA  LRTP
      MVI  B,7
      LXI  D,DATA
      LXI  H,PEAK
SCAT:LDAX D
      MOV  C,A
```

```
      CMP M
       BCAT
      JC ACAT
      JMP CCAT
BCAT: INX D
      INX H
      LDAX D
      CMP M
      JC ECAT
      JZ ECAT
      DCX H
      DCX D
CCAT: MOV M,C
      INX H
      INX D
      LDAX D
      MOV M,A
      JMP ECAT
ACAT: INX H
      INX D
ECAT: INX H
      INX D
DCAT: DCR B
      JNZ SCAT
      NOP
ERS:  NOP
      LXI H,TBBS
      SHLD TBBP
      XRA A
      STA ERRS
      MOV B,A
      LXI H,REFS
      LXI D,DATS
FERS: LDAX D
      CPI 77B
      MVI A,Ø
      JC BERS
      MVI A,377B
      NOP
BERS: CMP M
      JZ GERS
      MOV C,A
      PUSH D
      LXI D,FLGS
      MOV A,B
      ADD E
      MOV E,A
      LDAX D
      INR A
      CPI 3B
      JNZ DERS
      MVI A,Ø
      STAX D
      MOV M,C
      XCHG
      LHLD TBBP
      MOV M,B
      INX H
      SHLD TBBP
```

```
MPRH:LXI  D,FLGH
     MOV  A,E
     ADD  B
     MOV  E,A
     XRA  A
     STAX D
NPRH:POP  D
     INX  H
     INX  H
     INX  D
     INX  D
     INR  B
     MOV  A,B
     CPI  7B
     JNZ  SCPH
     NOP
 CPL:NOP
     XRA  A
     STA  ERRL
     MOV  B,A
     MOV  C,A
     LXI  D,DATA
     LXI  H,HLTL
 SCPL:LDAX D
     PUSH D
     CMP  M
     JNC  MPRL
     LXI  D,FLGL
     MOV  A,E
     ADD  B
     MOV  E,A
     LDAX D
     INR  A
     CPI  3
     JZ   PCL
     STAX D
     JMP  NPRL
 PCL:MVI  A,Ø
     STAX D
     PUSH H
     LXI  H,ERRL
     INR  M
     LXI  H,TABL
     MOV  A,C
     ADD  L
     MOV  L,A
     MOV  M,B
     INR  C
     POP  H
     JMP  NPRL
 MPRL:LXI  D,FLGL
     MOV  A,E
     ADD  B
     MOV  E,A
     XRA  A
```

```
      STAX D
NFRL:POP D
      INX H
      INX H
      INX D
      INX D
      INR B
      MOV A,B
      CPI 7B
      JNZ SCPL
      NOP
SBFR:NOP
      LDA ERRS
      MOV C,A
      ANA A
      JZ CFRM
      LHLD BSAF
      CALL LRTC
      SHLD BSAF
BFRM:LXI H,TABS
      SHLD TBBP
HFRM:DCR C
      JM CFRM
      LHLD TBBP
      MOV B,M
      INX H
      SHLD TBBP
      LXI H,REFS
      CALL CCWC
      JMP HFRM
CFRM:NOP
VBFR:LDA ERRH
      ANA A
      JZ ABFR
      LXI H,HLTH
      SHLD HDAK
      LXI H,PNTH
      LXI D,TABH
      CALL DOIT
      NOP
ABFR:LDA ERRL
      ANA A
      JZ TBFR
      LXI H,HLTL
      SHLD HDAK
      LXI H,PNTL
      LXI D,TABL
      CALL DOIT
      NOP
TBFR:LHLD TCNT
      INX H
      SHLD TCNT
      MOV A,L
      CPI 130B
      JNZ EXIT
      MOV A,H
      CPI 1
      JNZ EXIT
```

```
      LXI H,PNTH
      XRA A
ATOV:MOV M,A
      INX H
      DCR B
      JNZ ATOV
      LHLD BFAF
      CALL LRTC
      SHLD BFAF
      MVI C,Ø
CTOV:NOP
      MOV A,C
      CPI 7
      JZ BTOV
      LHLD BFAF
      CALL NFIL
      SHLD BFAF
      LXI H,DATA
      CALL MINR
      MVI M,15B
      INX H
      MVI M,12B
      INX H
      MVI M,44B
      SHLD BFAF
      INR C
      JMP CTOV
BTOV:LHLD BFAF
      MVI M,120B
      INX H
      MVI M,105B
      INX H
      MVI M,101B
      INX H
      MVI M,113B
      INX H
      MVI M,123B
      INX H
      MVI M,15B
      INX H
      MVI M,12B
      INX H
      MVI M,44B
      SHLD BFAF
      MVI C,Ø
DTOV:MOV A,C
      CPI 7B
      JZ EXIT
      LHLD BFAF
      CALL NFIL
      SHLD BFAF
      LXI H,PEAK
```

```
      CALL MINR
      MVI M,15B
      INX H
      MVI M,12B
      INX H
      MVI M,44B
      SHLD BFAF
      INR C
      JMP DTOV
ETOV:NOP
LXI1:POP PSW
      POP H
      POP D
      POP B
      EI
      NOP
      EI
      NOP
      RET
```

CONTINUED ON NEXT PAGE ----------

```
CNVT:NOP
     PUSH B
     MVI A,14B
     STA BCD
     LXI H,ABCD
     LXI B,0
HAI:MOV A,E
     RLC
     MOV E,A
     MOV A,D
     RAL
     MOV D,A
     JNC CON
     MOV A,C
     ADD M
     DAA
     MOV C,A
     MOV A,B
     INX H
     ADC M
     DAA
     MOV B,A
     JMP CONT
CON:INX H
CONT:INX H
     LDA BCD
     DCR A
     JZ OVER
     STA BCD
     JMP HAI
OVER:MOV H,B
     MOV L,C
     POP B
     HLT
ERPT:MVI C,105B
     CALL PRIN
     MVI C,122B
     CALL PRIN
     CALL PRIN
     MVI C,117B
     CALL PRIN
     MVI C,122B
     CALL PRIN
     MOV C,B
     CALL PRIN
     RET
PRIN:IN 12B
     ANA A
     JP PRIN
     MOV A,C
     OUT 13B
     RET
```

```
READ: IN  10B
      RLC
      JNC READ
      IN  11B
      OUT 13B
      ANI 177B
      MOV C,A
      RET
LETY: PUSH B
      MOV B,A
      RRC
      RRC
      RRC
      RRC
      ANI 17B
      ADI 60B
      MOV M,A
      INX H
      MOV A,B
      ANI 17B
      ADI 60B
      MOV M,A
      INX H
      POP B
      RET
CRAP: CALL READ
      MOV B,A
      CALL READ
      CALL PACK
      MOV M,A
      RET
PACK: MOV A,B
      RLC
      RLC
      RLC
      RLC
      ANI 360B
      MOV B,A
      MOV A,C
      ANI 17B
      ADD B
      RET
ZANG: PUSH B
      PUSH D
      PUSH H
      PUSH PSW
      CALL ZAMB
      POP PSW
      POP H
      POP D
      POP B
      RET
```

```
ZAMP:NOP
     LXI H,16000B
ZAMC:DI
     NOP
     MOV A,M
     CPI 44B
     JZ ZAMA
     INX H
     MOV C,A
     EI
EI   NOP
     NOP
     CALL PRIN
     JMP ZAMC
ZAMA:LXI H,16000B
     SHLD BFAS
     MVI M,44B
     RET
MOVT:LDAX D
     MOV M,A
     INX D
     INX H
     DCR B
     JNZ MOVE
     RET
MINR:NOP
     MOV A,C
     ADD C
     ADD L
     MOV L,A
     MOV D,M
     INX H
     MOV E,M
     CALL CNVT
     XCHG
     LHLD BFAF
     MOV A,D
     RRC
     RRC
     RRC
     RRC
     ANI 17B
     ADI 60B
     MOV M,A
     INX H
     MVI M,56B
     INX H
     MOV A,D
     ANI 17B
     ADI 60B
     MOV M,A
     INX H
     MOV A,E
     CALL LBTY
     NOP
     RET
```

```
NFIL:MOV A,C
     ADI 60B
     MOV M,A
     INX H
     MVI M,40B
     INX H
     MVI M,40B
     INX H
     NOP
     NOP
     RET
DOIT:NOP
     MOV B,A
     SHLD JBFR
BBFR:LDAX D
     INX D
     MOV C,A ;C ← VAR NO
     LHLD JBFR
     ADD L
     MOV L,A
     MOV A,M; ACC ← PNTH
     ANA A
     JNZ CHFR
     MVI M,377B
     LDA LRTP
     ANA A
     JNZ LOAD
     MVI A,377B
     STA LRTP
     NOP
     LHLD BFAF
     CALL LRTC
     SHLD BFAF
     NOP
LOAD:PUSH D
     [illegible]
     MOV M,P
     INX H
     LXI H,DATA
     CALL MINR
     NOP
     MVI M,126B
     INX H
     MOV M,P
     INX H
     MOV M,B
     INX H
     MVI M,44B
```

```
        SHLD BFAF
        LHLD HDAK
        CALL MINR
        MVI M,15B
        INX H
        MVI M,12B
        INX H
        MVI M,44B
        SHLD BFAF
        POP B
        POPD
        NOP
CBFR:   DCR B
        JNZ BFFR
        RET
LITC:   LXI D,TIMH
        LDAX D
        CALL LBTY
        DCX D
        LDAX D
        CALL LBTY
        MVI M,4CB
        INX H
        DCX D
        LDAX D
        CALL LBTY
        MVI M,15B
        INX H
        MVI M,12B
        INX H
        MVI M,44B
        RET
DRLG:   DI
        NOP
        LHLD BFAF
        CALL NFIL
        SHLD BFAF
        LXI H,FRZA
        CALL MINR
        MVI M,15B
        INX H
        MVI M,12B
        INX H
        MVI M,44B
        SHLD BFAF
        EI
        NOP
        EI
        NOP
        RET
CCWC:   MOV A,L
        ADD B
        MOV L,A
        MOV E,M
        MVI D,40B
        LHLD BSAF
        MOV A,B
        CPI 6B
```

```
        JNC  DFRM
        MVI  M,114B
        INX  H
        MVI  M,111B
        INX  H
        MVI  M,116B
        INX  H
        MVI  M,105B
        INX  H
        MOV  M,D
        INX  H
        MOV  A,B
        ADI  61B
        MOV  M,A
        INX  H
        MOV  M,D
        INX  H
        MOV  M,D
        INX  H
        MOV  A,E
        ANA  A
        JNZ  FFRM
        MVI  M,117B
        INX  H
        MVI  M,120B
        INX  H
        MVI  M,105B
        INX  H
        MVI  M,116B
        INX  H
        JMP  GFRM
FFRM:MVI  M,103B
        INX  H
        MVI  M,114B
        INX  H
        MVI  M,117B
        INX  H
        MVI  M,123B
        INX  H
        MVI  M,105B
        INX  H
        MVI  M,104B
        INX  H
GFRM:MVI  M,15B
        INX  H
        MVI  M,12B
        INX  H
        MVI  M,44B
        SHLD BSAF
        NOP
        JMP  HFRM
DFRM:MVI  M,107B
        INX  H
```

```
      MVI M,105B
      INX H
      MVI M,116B
      INX H
      MOV M,D
      INX H
      MOV M,D
      INX H
      MOV A,B
      ADI 53B
      MOV M,A
      INX H
      MOV M,D
      INX H
      MOV M,D
      INX H
      MVI M,117B
      INX H
      MOV A,E
      ANA A
      JZ JFRM
      MVI M,106B
      INX H
      MVI M,106B
      INX H
      JMP KFRM
JFRM:MVI M,116B
      INX H
KFRM:MVI M,15B
      INX H
      MVI M,12B
      INX H
      MVI M,44B
      SHLD RSAF
      JMP HFRM
CFRM:NOP
      NOP
      RET
GITA:NOP
      CALL PRIN
      CALL READ
      CPI 101B
      JNZ STAT
      LI
      NOP
      MVI B,20B
      LXI D,DATA
      LXI H,FRZA
      CALL MOVE
      EI
      NOP
      EI
      NOP
      MOV A,C
```

```
      OUT 13B
ROME: CALL READ
      CPI 44B
      JZ BLGM
      CPI 12B
      JZ GREK
      MOV A,C
      SUI 60B
      MOV C,A
      II
      NOP
      CALL DRLG
      II
      NOP
      EI
      NOP
      MOV A,C
      ADI 60B
      OUT 13B
      JMP ROME
HLGM: MVI C,0
VATN: DI
      NOP
      CALL DRLG
      EI
      NOP
      EI
      NOP
      INR C
      MOV A,C
      CPI 7B
      JZ VATN
      MVI A,44B
      OUT 13B
      RET
GRLK: MOV A,C
      NOP
      NOP
      OUT 13B
      RET
STAT: DI
      NOP
      MVI B,10B
      LXI D,REFS
      LXI H,FRZS
      CALL MOVE
      MOV A,C
      OUT 13B
      EI
      NOP
      EI
      NOP
```

```
SVRM:CALL RLAD
     CPI 44B
     JZ RGRM
     CPI 12B
     JZ GREK
     MOV A,C
     SUI 60B
     MOV B,A
     EI
     NOP
     LXI H,FRZS
     CALL CCWC
     MOV A,C
     OUT 13B
     EI
     NOP
     EI
     NOP
     JMP SVRM
RGRM:MVI B,0
CNTR:EI
     NOP
     LXI H,FRZS
     CALL CCWC
     INR B
     MOV A,B
     CPI 10B
     JNZ CNTR
     MOV A,C
     OUT 13B
     EI
     NOP
     EI
     NOP
     RET
```